**Lab S1: Special Topic of Electronics – MOSFET, CMOS Inverter**

**Objectives**

1. Understand the basic working principles of MOSET (metal oxide semiconductor field effect transistors), including both n-channel and p-channel MOS (NMOS and PMOS).
2. Explore the switching operations of NMOS and PMOS.
3. Explore the CMOS transistor digital circuits by constructing logic gates.

**Part 1: Working principles of NMOS and PMOS, and their switching operations**

The MOSFET being studied here is a three-terminal device. It includes a gate (G) terminal, a source (S) terminal, and a drain (D) terminal. It is possible to make current flow between the S and D terminals, since between S and D is a doped semiconductor substrate containing charge carriers (either electrons or holes). However, no current may flow through the G terminal, since the gate includes a layer of silicon dioxide, which is a non-conductive dielectric. **By controlling the voltage applied to the G terminal, you may control the conduction between S and D terminals by forming a channel under the gate G between the source S and the drain D. This is the working principle of MOSFET.** MOSFET that uses electrons as charge carriers is called n-channel MOS, or NMOS. MOSFET that uses holes as charge carriers is called p-channel NMOS, or PMOS.

Strictly speaking, a MOSFET has a fourth terminal – the bulk (B). However, in most MOSFET devices, this B terminal is connected (shorted) to the S terminal. The MOSFETs you explore here all have their S and B terminals connected together, as you can observe from the MOSFET circuit symbols below. See the table below for circuit symbols. In LTspice, a 3-terminal NMOS symbol is called nmos. A 4-terminal NMOS symbol is called nmos4. This naming convention is the same for PMOS devices.

NMOS and PMOS are duals. Here is a summary of these two types of MOSFET.

|  |  |  |
| --- | --- | --- |
|  | NMOS | PMOS |
| Charge carrier type | Electron (negative charge) | Hole (positive charge) |
| Conduction channel b/t S and D | n-channel | p-channel |
| Voltage to turn on transistor | Vgs (gate-to-source) | Vsg (source-to-gate) |
| High voltage rail is tied to | Drain terminal | Source terminal |
| Current flow direction | Drain to Source | Source to Drain |
| Circuit symbol |  |  |

**Part 1a: NMOS basic operation**

First, let’s explore the NMOS. For the NMOS, the charge carrier is electrons. When the **gate-to-source voltage** drop Vgs is below a **threshold** Vtn, no current may flow between D and S. When Vgs rises above Vtn, an electron channel (called the **n-channel**) forms under the gate between D and S, so current (called the **drain current** Id) will flow from D to S. The NMOS symbol has an arrow pointing toward the gate, signifying this n-channel.

Construct the following NMOS circuit. Note that the gate voltage Vg is obtained with a potentiometer (shown on LTspice as a combination of resistors R1 and R2). V1 signifies the power supply, and is set at 6V.

A diagram of a computer program

Description automatically generated

(1) Use the potentiometer to increase Vgs from zero to various higher levels (suggested to be at 0.1V intervals between 2.5V and 3.5V, and 0.5V or 1V intervals elsewhere). For each Vgs setting, *simultaneously* measure (using two DMMs) the drain current Id (flowing into the NMOS drain), and the drain-to-source voltage drop Vds. When Id stops increasing, you may end the measurements. Record the data for plotting.

(2) Plot Id vs. Vgs with Excel. Notice that as Vgs rises above the NMOS threshold voltage Vtn (somewhere around 2.5V), the drain current Id starts to increase rapidly, signifying the NMOS’s transition from non-conduction to full conduction. Beyond a certain Vgs (the saturation value, somewhere around 3.5V), the NMOS fully conducts, so the drain current Id does not increase further in any significant way. From the Id vs. Vgs plot, estimate both the threshold Vtn, and the saturation value of Vgs that make the NMOS fully conductive.

(3) Plot Vds vs. Vgs with Excel. Notice that when the NMOS starts to conduct, the drain-to-source voltage drop Vds decreases rapidly, signifying the NMOS’s transition from non-conduction to full conduction. When the NMOS fully conducts, Vds approaches zero, signifying full conduction.

Part 1: NMOS data table

|  |  |  |
| --- | --- | --- |
| Id vs. Vgs plot |  | |
| Vds vs. Vgs plot |  | |
| Threshold voltage Vtn (V) |  | |
| Full conduction Vgs (V) |  | |
| When Vgs is below Vtn, the NMOS is in what mode? (conduction/non-conduction) | |  |
| When NMOS is in non-conduction mode, it behaves like open or short circuit? | |  |
| When Vgs is above Vtn, the NMOS is in what mode? (conduction/non-conduction) | |  |
| When NMOS is in full conduction mode, it behaves like open or short circuit? | |  |

**Part 1b: PMOS basic operation**

Now that you have explored the NMOS, let’s explore the PMOS, which is the dual of the NMOS. For the PMOS, the charge carrier is holes (the dual of electrons). The high voltage rail (the ground rail in this circuit) is connected to the S terminal of the PMOS. The D terminal of the PMOS is connected to a low voltage rail (-10V in this circuit). To turn on the PMOS so that it conducts, a source-to-gate voltage Vsg must be increased to above a threshold Vtp. As the PMOS starts conducting current, the current Id will flow from S to D.

Construct the following PMOS circuit. Note that the low voltage rail Vdd is obtained directly from the power supply (by grounding the red terminal of Channel 1 and taking the black terminal as the low volage rail). Also note that the gate voltage Vg is again obtained with a potentiometer (shown on LTspice as a combination of resistors R1 and R2).

A diagram of a program

Description automatically generated

(1) Use the potentiometer to increase Vsg from zero to various higher levels (suggested to be at 0.1V intervals between 3V and 4V, and 0.5V or 1V intervals elsewhere). For each Vsg setting, *simultaneously* measure (using two DMMs) the drain current Id (flowing out of the PMOS drain), and the source-to-drain voltage drop Vsd. When Id stops increasing, you may end the measurement. Record the data for plotting.

(2) Plot Id vs. Vsg with Excel. Notice that as Vsg rises above the PMOS threshold voltage Vtp (somewhere around 3V), the drain current Id starts to increase rapidly, signifying the PMOS’s transition from non-conduction to full conduction. Beyond a certain Vsg (the saturation value, somewhere around 4V), the PMOS fully conducts, so the drain current Id does not increase further in any significant way. From the Id vs. Vsg plot, estimate both the threshold Vtp, and the saturation value of Vsg that makes the PMOS fully conductive.

(3) Plot Vsd vs. Vsg with Excel. Notice that when the PMOS starts to conduct, the source-to-drain voltage drop Vsd decreases rapidly, signifying the PMOS’s transition from non-conduction to full conduction. When the PMOS fully conducts, Vsd approaches zero, signifying full conduction.

Part 1: PMOS data table

|  |  |  |
| --- | --- | --- |
| Id vs. Vsg plot |  | |
| Vsd vs. Vsg plot |  | |
| Threshold voltage Vtp (V) |  | |
| Full conduction Vsg (V) |  | |
| When Vsg is below Vtp, the PMOS is in what mode? (conduction/non-conduction) | |  |
| When PMOS is in non-conduction mode, it behaves like open or short circuit? | |  |
| When Vsg is above Vtp, the PMOS is in what mode? (conduction/non-conduction) | |  |
| When PMOS is in full conduction mode, it behaves like open or short circuit? | |  |

**Part 2: Digital applications – CMOS logic gates**

CMOS refers to complementary MOS, which means both the NMOS and its dual PMOS are used in the same circuit. Circuits employing CMOS logic gates is the workhorse of modern digital IC (Integrated Circuits).

**Logic inverter (NOT gate)**

The simplest CMOS digital circuit is an inverter, and it achieves the logic function of NOT. Here is the circuit symbol of a logic inverter (the triangle mean buffer; he small circular bubble means inversion):

Diagram

Description automatically generated

Here is the truth table of a NOT function (logic inverter)

|  |  |
| --- | --- |
| Input a | Output f = NOT(a) |
| 0 | 1 |
| 1 | 0 |

The 0 and 1 in the above truth table are logic 0 and logic 1. They correspond to a low voltage and a high voltage, respectively. In this lab, we will use LEDs to display these logic values. Logic 0 means the LED is off; logic 1 means the LED is on.

Using one NMOS and one PMOS (as well as a sliding switch, two LEDs, and a resistor), construct the following CMOS inverter circuit. The input switch is a sliding switch that is a single pole double throw (SPDT) switch.

Pay very close attention to how you connect the gate (G), the source (S), and the drain (D) of both the NMOS and the PMOS. Particularly, the drains of the NMOS and PMOS should be connected together to form the output node f. The gates of the NMOS and PMOS should be connected together to form the input node a. The PMOS source should be connected to the high voltage rail (5V). The NMOS source should be connected to the low voltage rail (ground). The input indicator should be an LED (red or some other color), and is connected between the input node and the ground. This LED must be protected by a 1k resistor in series (a crucial thing to do). The output indicator should be another LED (green or some other color, but the input and output LEDs should have different colors to avoid confusion), and is connected between the output node and the ground. This LED must beprotected by a 1k resistor in series (a crucial thing to do). Without protective resistors, the LEDs may be damaged. On the other hand, if the LED lighting is too dim, reduce the protective resistor’s value from 1k to 0.2k, or even less.

Diagram, schematic

Description automatically generated

To input a logic 1, toggle the input switch to the 5V power rail. To input a logic 0, toggle the input switch to the ground rail. Notice how the circuit design uses LEDs to explicitly display the logic values of the input and output. **In general, if you want to use an LED to display the logic value of a node, simply connect that node to the LED and a protective resistor in series, and then to the ground.** If the node experiences a high voltage, the LED will be turned on. If the node experiences a low voltage, the LED will be turned off. Each protective resistor protects the LED by limiting the current flowing through the LED.

Operate the CMOS inverter circuit, and compare the results to the truth table of the NOT function to verify that you have indeed achieved the NOT function.

To help you understand how the CMOS inverter works, toggle the input switch to 0V (ground), and determine the conduction paths based on the conduction mode of the NMOS and the conduction mode of the PMOS. Convince yourself that the input node a is at 0V (hence a logic value of 0), and the output node f is at 5V (hence a logic value of 1). Now toggle the input switch to 5V (power rail), and perform the same circuit analysis. To help you organize your thought process, fill out the following data table.

Part 2: CMOS inverter working principles

|  |  |  |
| --- | --- | --- |
| Input node a’s logic value |  |  |
| Input switch togged to 0V or 5V? |  |  |
| Input node a’s voltage = 0V or 5V? |  |  |
| Input LED is on or off? |  |  |
| NMOS Vgs = 0V or 5V? |  |  |
| NMOS is conductive/non-conductive? |  |  |
| Output node f is shorted to ground (Y/N)? |  |  |
| PMOS Vsg = 0V or 5V? |  |  |
| PMOS is conductive/non-conductive? |  |  |
| Output node f is shorted to 5V power rail (Y/N)? |  |  |
| Output node f’s voltage = 0V or 5V? |  |  |
| Output LED is on or off? |  |  |
| Output node f’s logic value f = 0 or 1? |  |  |

**Data tables**

Part 1: NMOS data table

|  |  |  |
| --- | --- | --- |
| Id vs. Vgs plot |  | |
| Vds vs. Vgs plot |  | |
| Threshold voltage Vtn (V) |  | |
| Full conduction Vgs (V) |  | |
| When Vgs is below Vtn, the NMOS is in what mode? (conduction/non-conduction) | |  |
| When NMOS is in non-conduction mode, it behaves like open or short circuit? | |  |
| When Vgs is above Vtn, the NMOS is in what mode? (conduction/non-conduction) | |  |
| When NMOS is in full conduction mode, it behaves like open or short circuit? | |  |

Part 1: PMOS data table

|  |  |  |
| --- | --- | --- |
| Id vs. Vsg plot |  | |
| Vsd vs. Vsg plot |  | |
| Threshold voltage Vtp (V) |  | |
| Full conduction Vsg (V) |  | |
| When Vsg is below Vtp, the PMOS is in what mode? (conduction/non-conduction) | |  |
| When PMOS is in non-conduction mode, it behaves like open or short circuit? | |  |
| When Vsg is above Vtp, the PMOS is in what mode? (conduction/non-conduction) | |  |
| When PMOS is in full conduction mode, it behaves like open or short circuit? | |  |

Part 2: CMOS inverter working principles

|  |  |  |
| --- | --- | --- |
| Input node a’s logic value |  |  |
| Input switch togged to 0V or 5V? |  |  |
| Input node a’s voltage = 0V or 5V? |  |  |
| Input LED is on or off? |  |  |
| NMOS Vgs = 0V or 5V? |  |  |
| NMOS is conductive/non-conductive? |  |  |
| Output node f is shorted to ground (Y/N)? |  |  |
| PMOS Vsg = 0V or 5V? |  |  |
| PMOS is conductive/non-conductive? |  |  |
| Output node f is shorted to 5V power rail (Y/N)? |  |  |
| Output node f’s voltage = 0V or 5V? |  |  |
| Output LED is on or off? |  |  |
| Output node f’s logic value f = 0 or 1? |  |  |